RF Performance of Planar III–V Nanowire-Array Transistors Grown by Vapor–Liquid–Solid Epitaxy

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Abstract—The radio frequency (RF) performance of a III–V transistor comprised of nanowire (NW) high-electron mobility channels, grown by planar vapor–liquid–solid epitaxy in parallel arrays, is examined. An equivalent small-signal circuit model was used to study the contributing extrinsic and intrinsic passive elements on the NW performance as a function of bias and gate length (L_G). Adequate intrinsic gain (g_m/g_{ds}) ~25 with low intrinsic (R_i) and terminal resistances (R_G, R_S, R_D) lead to an f_T/f_{max} ~ 30/78 GHz for L_G = 150 nm and NW diameter ~160 nm. The gate capacitance (C_g) is extracted and ~2/3 of the total C_g is parasitic, which can be reduced with denser NW arrays. Excellent agreement between measured and modeled RF performance is achieved.

Index Terms—Nanowire, parallel-array, radio frequency, transistor, small-signal model, vapor-liquid-solid.

I. INTRODUCTION

III-V NANOWIRES (NWs) for electronic devices are emerging due to their inherent three-dimensional (3D) geometry, which can be utilized as a multiple gate, high-mobility channel with enhanced electrostatic gate-channel coupling [1]. Attention has especially been given to NWs grown by metal-seeded vapor-liquid-solid (VLS) epitaxy as this eliminates damage from top-down etching. Immediate benefits of III-V NWs, so far, have focused on improved static performance over conventional transistors [2]–[7]. Realizing high-speed NW performance requires densely packed arrays of NWs aligned in parallel so that the overall intrinsic gate capacitance ($C_{g,i}$) is large compared to the total parasitic capacitance ($C_{g,p}$) [8]. By doing so, high-speed 3D NW channels with enhanced electrostatics are candidates for future RF nanoelectronics with high maximum oscillating frequency (f_{max}) [9]. However, the practical challenges of

NW assembly have resulted in low f_{max}, and the RF behavior of nanoscale channels has been left largely unexplored. For example, the record RF speed for laterally aligned InAs and silicon VLS NWs is 1.8 GHz [5] and 0.34 MHz [10], respectively, while the best carbon nanotube transistor has reached just 30 GHz [11]—all far below their theoretical potential. Major contributing factors for low f_{max} include the fringing fields of the gated regions between NWs, which do not conduct in the on-state but still contribute to $C_{g,p}$. One solution is to leave dense arrays of VLS NWs in their preferred out-of-plane growth direction, but this creates high pad capacitance from overlapping transistor terminals [4]. Alternatively, an f_{max} exceeding 300 GHz with 32-nm gate length (L_G) has also been achieved with III-V non-planar channels aligned in the substrate plane via selective regrowth [12]. In that case, the channel geometry depends on top-down lithography; whereas, bottom-up NWs grown by VLS method require patterning only the metal seed nanoparticle.

Recently, we reported wafer-scale assembly of high-speed, defect-free planar NWs as high-electron mobility transistor (HEMT) channels, grown self-aligned in dense, parallel arrays along the substrate surface by the planar VLS method [13]. In this letter, we present an in-depth study of the RF performance and use a small-signal equivalent circuit model (SSM) to investigate the limiting and contributing factors for high f_{max} using planar-array NW-HEMT channels. RF characterization of NW-HEMTs as a function of L_G and bias are discussed in detail.

II. DEVICE FABRICATION AND RF MEASUREMENTS

Two-finger AlGaAs/GaAs NW-HEMT devices were grown and fabricated on a (100) semi-insulating (SI) GaAs wafer using a process described in [13] and [14]. For this sample, the NW diameter is ~160 nm with 300-nm patterned NW center pitch. As illustrated in Figs.1(a)-(c), the GaAs NWs grow bi-directionally on this substrate orientation so only about half of the parallel NWs are used for the HEMT fabrication. The number of NWs per device is ~25, each of which spans across both sides of the double channels; and the T-gate L_G varies from 150-300 nm in 50 nm increments. For L_G = 150 nm and V_{DS} = 2 V, the dc metrics are 0.2 mA/μm maximum drain current, 0.35 mS/μm peak transconductance ($g_{m,peak}$), I_{ON}/I_{OFF} ~ 10^4, V_{TH} ~ +0.2 V, SS ~ 102 mV/dec and $DIBL$ ~ 140 mV/V [13].

RF performance was characterized with an Agilent E8364B parametric analyzer equipped with bias tees for dc bias. Scattering (S-) parameters for each device were measured at various gate and drain bias in the 0.01-40 GHz range
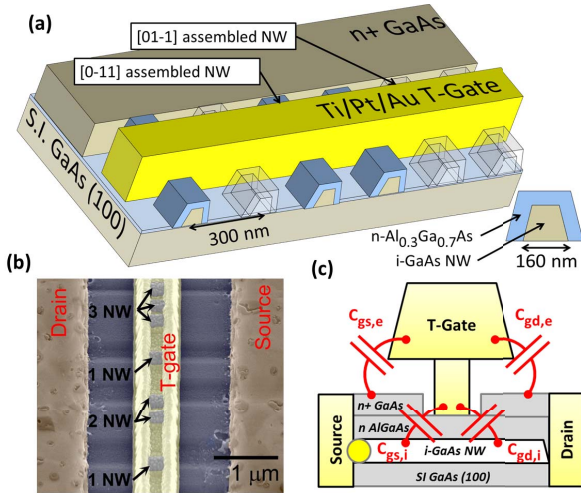
Fig. 1. (a) NW-HEMT device schematic in the gate recess region depicting the bi-directional VLS GaAs NW self-assembly on SI GaAs (100) substrate. Approximately half of the NWs are used for transistor fabrication. (b) Magnified top-view false color SEM of the NW-HEMT channel region. (c) A capacitive diagram of the NW-HEMT illustrating both extrinsic and intrinsic gate capacitance.
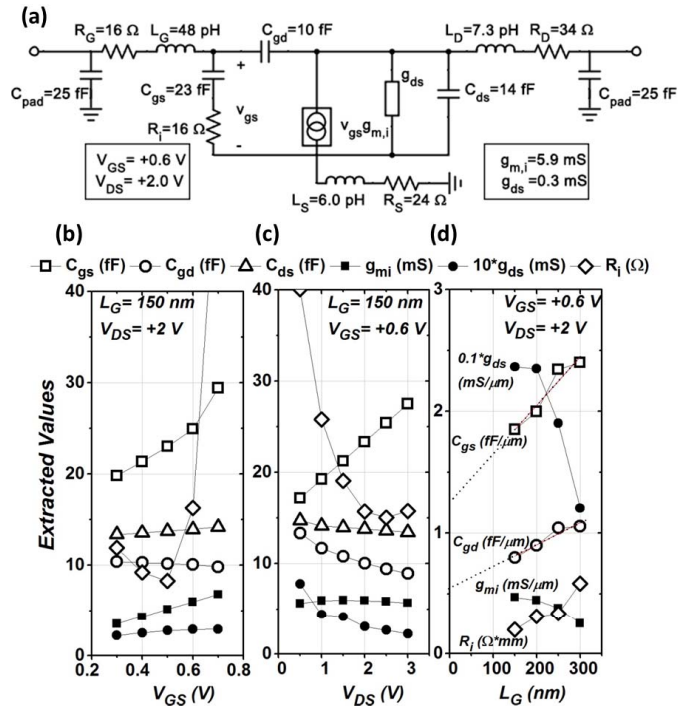

Fig. 2. (a) SSM for the fabricated NW-HEMT devices with approximately ~25 NWs each. The extracted values shown are for $L_G = 150$ nm at a bias of $V_{GS}/V_{DS} = +0.6/2.0$ V. (b)-(d) Influential extracted SSM parameters for high f_{max} as a function of V_{GS}, V_{DS} and L_G. In (d), the values are normalized to the total NW width.

at −27 dBm power. Calibration to the RF probe tips was accomplished by short-open-load-thru routine with an off-chip substrate standard. Extrinsic pad delay was de-embedded with on-wafer open and short devices which resemble an identical NW-HEMT without the NWs and mesa.

III. RF MODEL AND RESULTS

The SSM illustrated in Fig.2(a) was used to examine the limiting and contributing factors for high-speed operation. Three bias conditions were used to isolate the extrinsic and intrinsic elements—(*i*) cold bias ($V_{GS}/V_{DS} = -2/0$ V), (*ii*) zero-bias ($V_{GS} = V_{DS} = 0$ V) and (*iii*) hot bias ($V_{GS}/V_{DS} = +0.6/2$ V). The extraction routine is the same as for conventional Schottky-gated III-V HEMTs, which uses a least squares fit after calculating an accurate starting estimate [15]. After determining the extrinsic components, the intrinsic circuit elements were analytically calculated. The resulting SSM values for $V_{GS} = +0.6$ V and $V_{DS} = +2$ V are displayed in Fig. 2(a).

Figs.2(b)-(d) illustrate the variation of extracted SSM parameters as a function of V_{GS}, V_{DS} and L_G, respectively. The gate capacitances, C_{gs} and C_{gd}, are greatly affected by both drain and gate bias because of the close proximity of the gate-recessed n$^+$ GaAs cap to the T-gate stem, just tens of nanometers as confirmed by cross-sectional scanning electron microscopy (SEM). The source and drain access resistance (R_S, R_D) was in the range of 25-35 Ω for the studied L_G range. The R_S is excellent considering the extracted intrinsic transconductance, $g_{m,i} \sim$ 3-6 mS, results in $R_S \cdot g_{m,i} \ll 1$ and the measured transconductance, $g_m = g_{m,i}/(1 + R_S \cdot g_{m,i})$, is not greatly affected. Low Ti/Pt/Au T-gate resistance (R_G) increased incrementally from 100-188 Ω·μm as L_G decreased. The intrinsic resistance (R_i) was the most volatile parameter which followed closely with the gate diode leakage. For example, R_i was the highest as V_{DS} and V_{GS} approached 0 V and +0.7 V, respectively, which

is the two-terminal bias condition for forward-bias Schottky gate leakage. The optimal R_i occurs when the electron channel is formed at higher V_{DS} but with $V_{GS} < +0.7$ V to prevent the gate diode from turning on. The output conductance, g_{ds}, remains low for the entire biasing range, which is due to the excellent electrostatics afforded by the 3D NW channel multi-gate. The intrinsic gain, $g_o = g_{m,i}/g_{ds}$, an important figure of merit for high f_{max} (Fig.3(a)) clearly shows improvement with V_{DS}. For $L_G = 150$ nm, a high $g_o \sim 25$ was extracted. The significance of low terminal and intrinsic resistances combined with low output conductance for high f_{max} is given by eq.(1) below:

$$f_{max} = \frac{f_T}{2\sqrt{g_{ds}(R_G + R_i + R_S) + 2\pi f_T R_G C_{gd}}}$$
$$\propto \frac{g_m}{\sqrt{g_m + g_{ds}}} \tag{1}$$

The current gain cutoff frequency, $f_T \approx g_m/(2\pi C_g)$, requires large g_m/C_g ratio where $C_g = C_{g,i} + C_{g,e}$ and $C_{g,e}$ is the extrinsic fringing gate capacitance. Both $C_{g,i}$ and $C_{g,e}$ can be separated into gate-source ($C_{gs,i}$ and $C_{gs,e}$) and gate-drain ($C_{gd,i}$ and $C_{gd,e}$) components as illustrated in Fig.1(c).

For the $L_G = 150$ nm NW-HEMT device, the $C_{g,i}$ and $C_{g,e}$ were extracted and analyzed. The L_G-independent $C_{g,e}$ can be extracted from the intercept of a C_g versus L_G plot in Fig.2(d). For each gated device, the C_g is normalized by taking the three-sided gated perimeter of each NW multiplied by the number of NWs. $C_{gs,e}$ and $C_{gd,e}$ were found to be 15.8 fF and 6.8 fF, respectively. The slope of C_{gs} and C_{gd} versus L_G defines the L_G-dependent elements, $C_{gs,i}$ and $C_{gd,i}$, which
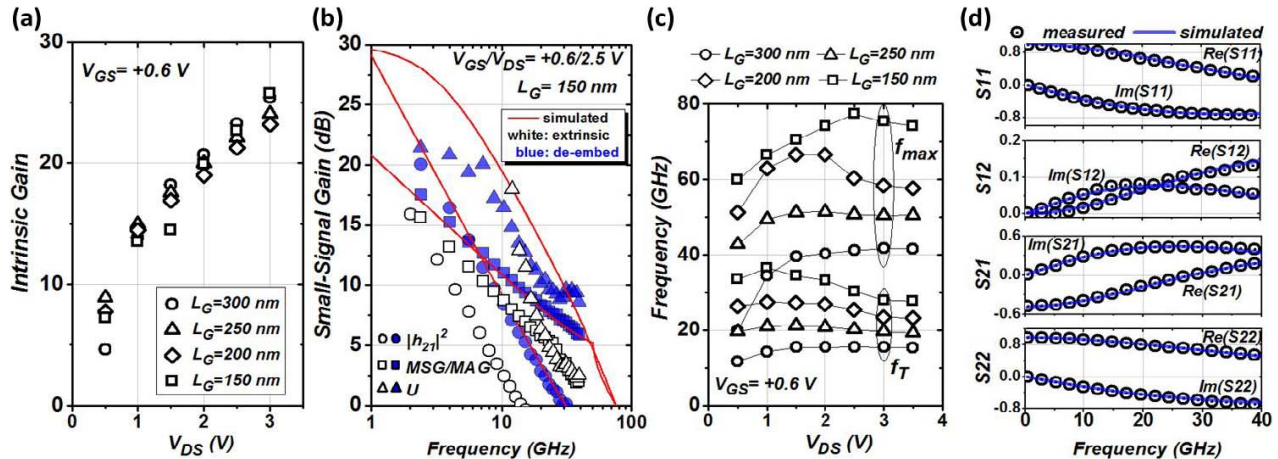
Fig. 3. (a) Intrinsic gain of the NW-HEMT device for various L_G and V_{DS}. (b) Representative extrinsic and de-embed RF gain performance for $L_G = 150$ nm and $V_{GS}/V_{DS} = +0.6/2.5$ V. (c) De-embed RF performance versus V_{DS} and L_G at $V_{GS} = +0.6$ V. (d) Excellent agreement between simulated and measured S-parameters is achieved using the values shown in the previously shown SSM circuit.

are 7.5 fF and 3.5 fF, respectively. When comparing these values to the total extracted C_{gs} and C_{gd} in Fig.2(c), we find $C_{gs,i}/C_{gs}$ and $C_{gd,i}/C_{gd}$ are 33% and 35%, respectively. In other words, ~2/3 of the total extracted C_g is parasitic. Most of $C_{g,p}$ is likely caused by the bi-directional VLS NW growth which can be optimized on (110) GaAs substrate orientation for uni-directional NW assembly and immediately enhance the g_m/C_g ratio for higher f_T/f_{max} [16].

The SSM values were used to simulate the maximum available and stable gains (MAG/MSG) and the de-embedded f_T and f_{max}. Fig.3(b) shows representative measured and de-embedded small-signal gain performance for $L_G = 150$ nm at $V_{DS} = +2.5$ V. Fig. 3(c) illustrates the dependence of f_T and f_{max} as a function of L_G and V_{DS}. The optimum f_T occurs at $V_{DS} = +1$ V, which is just beyond the saturation V_{DS}. For higher V_{DS}, the drain-side electric field degrades f_T likely because of impact ionization onset but also widens the drain depletion region to lower C_{gd} and increase f_{max}. The best frequency performance was measured at $V_{DS} = +2.5$ V with $f_T/f_{max} \sim 30/78$ GHz for $L_G = 150$ nm. An $f_{max} \cdot L_G \sim 11.7$ GHz·μm is the best reported among all NW and nanotube transistors [4], [5], [11], [12]. The total intrinsic delay, τ_i, can be estimated by $C_{g,i}/g_{m,i} = 1.86$ ps, and the corresponding electron velocity, v_e, is $L_G/\tau_i = 0.8 \cdot 10^7$ cm/s. Removing the fringing capacitance, a theoretical f_T can be determined by $(2\pi \cdot \tau_i)^{-1} = 85$ GHz. Using $f_{max} \approx [f_T/(8\pi \cdot R_G \cdot C_{gd,i})]^{0.5}$, a theoretical $f_{max} = 248$ GHz is calculated for the NW-HEMT device with $L_G = 150$ nm. Outstanding agreement between the measured S-parameters and the simulated S-parameters developed from Fig.2(a) is shown in Fig.3(d) and validates the SSM extraction process.

IV. Conclusion

The RF performance and SSM of a III–V NW-HEMT with densely aligned parallel AlGaAs/GaAs NWs have been presented. The NW-HEMT array has the highest $f_{max} = 78$ GHz reported for VLS NWs aligned along the substrate surface. The high f_{max} is attributed to low device resistance and good intrinsic gain. High $C_{g,p}$ limiting

RF performance can be improved with device engineering and unidirectional planar VLS NW growth on future samples.

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